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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,375	03/12/2004	Vijay K.G. Sindagi	TI-35832	7298

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EXAMINER	
MOLL, JESSE R	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 10/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,375	SINDAGI ET AL.	
	Examiner	Art Unit	
	Jesse R. Moll	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,5 and 7-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5 and 7-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
9/18/2006

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 2, 4, 5 and 7-11 have been examined.

Acknowledgment of papers filed: amendment filed 19 July 2006. The papers filed have been placed on record.

Withdrawn Objections

2. Applicant, via amendment has overcome the objections to claim 1, 2, 4, 5 and 7. The objections have been respectfully withdrawn.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1, 2, 8 and 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "an instruction decode pipeline phase" in lines 8 and 9. It is unclear as to whether this refers to the previous mention of "an instruction

decode pipeline phase" recited in lines 2 and 3. Examiner suggest the limitation read "said instruction decode pipeline phase".

Claims 2, 8 and 9 are rejected due to their dependence on indefinite claim 1.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2, 4, 5 and 7-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kling (U.S. Patent No. 6,883,089 B2) in view of Yamada et al. (U.S. Patent No. 6,877,087 B1) herein referred to as Yamada.

7. Regarding claim 1, Kling discloses a pipelined data processor capable of predicated instruction execution dependent upon the state of an instruction designated predicate register comprising: a data register file (Register File 168, see figs. 1A and 1B) including a plurality of read/write, general purpose data registers (see col. 3, lines 15 and 32); an instruction decode unit (Front end 160 and Register read 162)

Note that the term "decode unit" merely claims a device which decodes instructions. Therefore, the section of the processor which performs the register read and the front end in combination are considered to be a decode unit.

Operative during an instruction decode pipeline phase

Note that the definition of the word "phase" according to The American Heritage® Dictionary of the English Language, Fourth Edition is "An aspect; a part". Therefore, any phase in which the decode unit performs operations on an instruction is considered to be the instruction decode pipeline phase.

Receiving fetched instructions (see col. 3, lines 13-15) and determining the identity of at least one source operand data register (see col. 3, line 15), a destination operand data register (see col. 3, line 31-32) and one of a plurality of functional units for execution (see col. 2, lines 26-27 and 35-36) of each instruction, said instruction decode unit further identifying a predicate register (Scoreboard 170, see figs. 1A and 1B; col. 2, lines 46-50) responsive to receipt of a predicated instruction (see col. 3, lines 18-24); the plurality of functional units operative during an execution pipeline phase

Note that the definition of the word "phase" according to The American Heritage® Dictionary of the English Language, Fourth Edition is "An aspect; a part". Therefore, any phase in which the functional unit performs operations on an instruction is considered to be the instruction execution pipeline phase.

Connected to said instruction decode unit for performing a data processing operation (see col. 2, lines 26-29) on at least one source operand recalled from at least one corresponding instruction designated source data register (see col. 3, line 15) and

producing a result (result; see col. 2, lines 52-55), said functional unit responsive to a predicate instruction (see col. 2, lines 54-55) to write said result to an instruction designated destination data register if said corresponding predicate data register has a first state (true) and to nullify said instruction (discarding the instruction) and not write said result if said predicate register has a second state opposite to said first state (false; see col. 3, lines 29-33); a scoreboard bit (if the operand is available) corresponding to each data register capable of serving as a predicate register (see col. 3, lines 16-21), each scoreboard bit connected to said instruction decode unit (see fig. 1A and 1B) to be set to a first digital state (not available) upon determining said corresponding data register is a destination for an instruction

Note that the operands are not available until the instruction is executed, therefore an indication must be set to show that the operand is not available. Since the processor checks this condition, it must be stored.

And connected to said plurality of functional units to be reset to a second digital state (available) opposite to said first digital state upon functional unit write of a result to said corresponding data register;

Note that the operands are not available until the instruction is executed, therefore an indication must be set to show that the operand is available when it is executed. Since the processor checks this condition, it must be stored.

And each functional unit is further operative responsive to a predicate instruction during the decode pipeline phase to nullify said predicate instruction (see col. 3, lines 9-12; col. 4, lines 31-45)

Note that the value of the predicate and scoreboard can be known in when the registers are read (decode phase; see above). Therefore, the instruction would be discarded in the decode phase.

Of a following execution phase (instruction that would have been executed in a following phase) if said predicate register has said second state and said corresponding scoreboard bit has said second state (see col. 3, lines 40-42).

Kling does not expressly disclose nullifying said predicate instruction by operating at a reduced power state relative to normal instruction operation.

Yamada teaches nullifying instructions by operating at a reduced power state relative to normal instruction operation (see column 5, lines 46-54).

It would have been obvious at the time of the invention for one of ordinary skill in the art to have modified the invention of Kling by nullifying instructions by operating at a reduced power state relative to normal instruction operation, as taught by Yamada, in order to conserve power (see column 5, lines 46-49).

8. Regarding claim 2, Kling discloses the pipelined data processor of claim 1, wherein: said functional unit is further operative to reset said scoreboard bit to said second digital state upon nullification of said instruction designating a corresponding data register as a destination operand data register.

Note that the processor must update the scoreboard in response to nullifying an instruction. If the scoreboard is not updated, the processor could stall indefinitely waiting for operands to become available.

9. Claims 4-6 recite equivalent limitations as claims 1-3 respectively and are therefore anticipated by the method the processor of Kling uses (see above regarding claims 1-3).

10. Regarding claim 7, Kling discloses the method of claim 4 further comprising the steps of: statically scheduling instruction execution via a compiler (compiling code; when machine code is generated, instructions are scheduled to execute in program order; see fig. 2) and scheduling via said compiler a last write (instruction 3; see fig. 3) to a data register (P1; see fig. 2) before a decode phase of a predicate instruction (instruction 4) designating said data register as a predicate register (certainly the compiler will schedule the instructions [create the program order] prior to the program being run on a processor [where the decode phase occurs]).

11. Regarding claim 8, Kling discloses the pipelined data processor of claim 1.

Kling does not expressly disclose that each functional unit is operable at said reduced power state by not fetching at least one instruction operand and not toggling a corresponding register read port during said following execution phase.

Yamada teaches functional units operable at said reduced power state by not fetching at least one instruction operand (from register 21; see figs 1 and 6) and not toggling a corresponding register read port during said following execution phase (see col. 6, lines 49-59 regarding not reading data to latch 22).

It would have been obvious at the time of the invention for one of ordinary skill in the art to have modified the invention of Kling by not fetching at least one instruction operand and not toggling a corresponding register read port, as taught by Yamada, in order to conserve power (see column 6, lines 57-59).

12. Regarding claim 9, Kling discloses the pipelined data processor of claim 1.

Kling does not expressly disclose each functional unit is operable at said reduced power state by not powering said functional unit during said following execution phase.

Yamada teaches functional units operable at said reduced power state by not powering said functional unit during said following execution phase (see col. 8, lines 30-33).

It would have been obvious at the time of the invention for one of ordinary skill in the art to have modified the invention of Kling by not powering said functional unit during said following execution phase, as taught by Yamada, in order to conserve power (see col. 9, lines 3-7).

13. Claims 10 and 11 recite equivalent limitations as claims 8 and 9 and are rejected under the same grounds.

Response to Arguments

14. Applicant's arguments with respect to claims 1, 4, and 7-11 have been considered but are moot in view of the new ground(s) of rejection. See above for detailed analysis of the claims.

15. Regarding the arguments directed at claims 2 and 5, Examiner disagrees. Examiner's statement in the previous Office Action was merely to show that the apparatus of Kling **MUST** reset said scoreboard bit to said second digital state upon nullification of said instruction. If this does not occur, the pipeline would stall indefinitely and normal operation could not continue. Examiner asserts that this feature is inherent in the invention of Kling. If an instruction writing to the predicate bit is nullified, the scoreboard **MUST** be updated to allow execution of dependent instructions.

Conclusion

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse R. Moll whose telephone number is (571)272-2703. The examiner can normally be reached on M-F 9:00 am - 5:30 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on 571-272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jesse R Moll
Examiner
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JM 9/27/06

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